

1 38. The cache coherency system of claim 36, said memory
2 controller further being selectively operable for deleting a
3 cache line from said cache at said first node when said
4 cache is full to provide space for a new cache line to be
5 stored to said cache, and for sending the address of the
6 deleted cache line to an invalidation directory to indicate
7 said node no longer has a copy of said cache line.

1 39. The cache coherency system of claim 36, said memory
2 controller further being selectively operable for sending
3 cache update messages to update corresponding cache lines at
4 all remote nodes having copies of a changed cache line and
5 for receiving cache lines of data from remote nodes for
6 updating the cache at said first node.

Ab
could.

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REMARKS

In the parent application, the Examiner required restriction to one of four groups of claims. Applicant selected to prosecute the claims of Group III in the parent application, and this application is filed with respect to

claim 1, the sole claim in Group I which, as the Examiner characterizes it is drawn to a cache coherency system. Applicants have added additional claims 31-39, also drawn to cache coherency systems, methods of operating cache coherency systems, and corresponding Beauregard style claims.

A clean copy of a replacement Abstract page is appended hereto.

SUMMARY AND CONCLUSION

Applicant urges that the above amendments be entered and the case passed to issue with claims 1, and 31-39.

If, in the opinion of the Examiner, a telephone conversation with applicant(s) attorney could possibly

facilitate prosecution of the case, he may be reached at the number noted below.

Sincerely,

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By

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